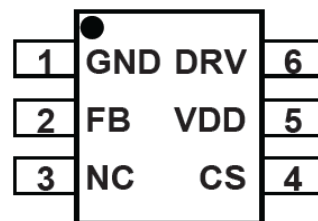


[illegible]

The block diagram illustrates the internal architecture of the PMIC. Key components include:

- Power Input:** VDD (Pin 5) and GND (Pin 1).
- Power Regulation:** A **Startup** block and an **LDO** (Low Dropout Regulator) providing a **5V** output.
- Control and Monitoring:**
 - Logic Controller:** The central control unit.
 - Gate Drive:** Receives signals from the Logic Controller to drive the **DRV** (Pin 6).
 - OCP (Over-Current Protection):** Receives signals from the Logic Controller and provides feedback to the **CS** (Pin 4).
 - Leading Edge Blanking:** Receives signals from the OCP.
 - Protection:** Receives signals from the Logic Controller.
- Timing and Feedback:**
 - Clock Generator:** Provides a clock signal to the Logic Controller.
 - PWM CMP (Pulse Width Modulation Comparator):** Receives feedback from the **FB** (Pin 2) and provides a signal to the Logic Controller.
- Other Pins:**
 - NC (Pin 3):** No Connection.

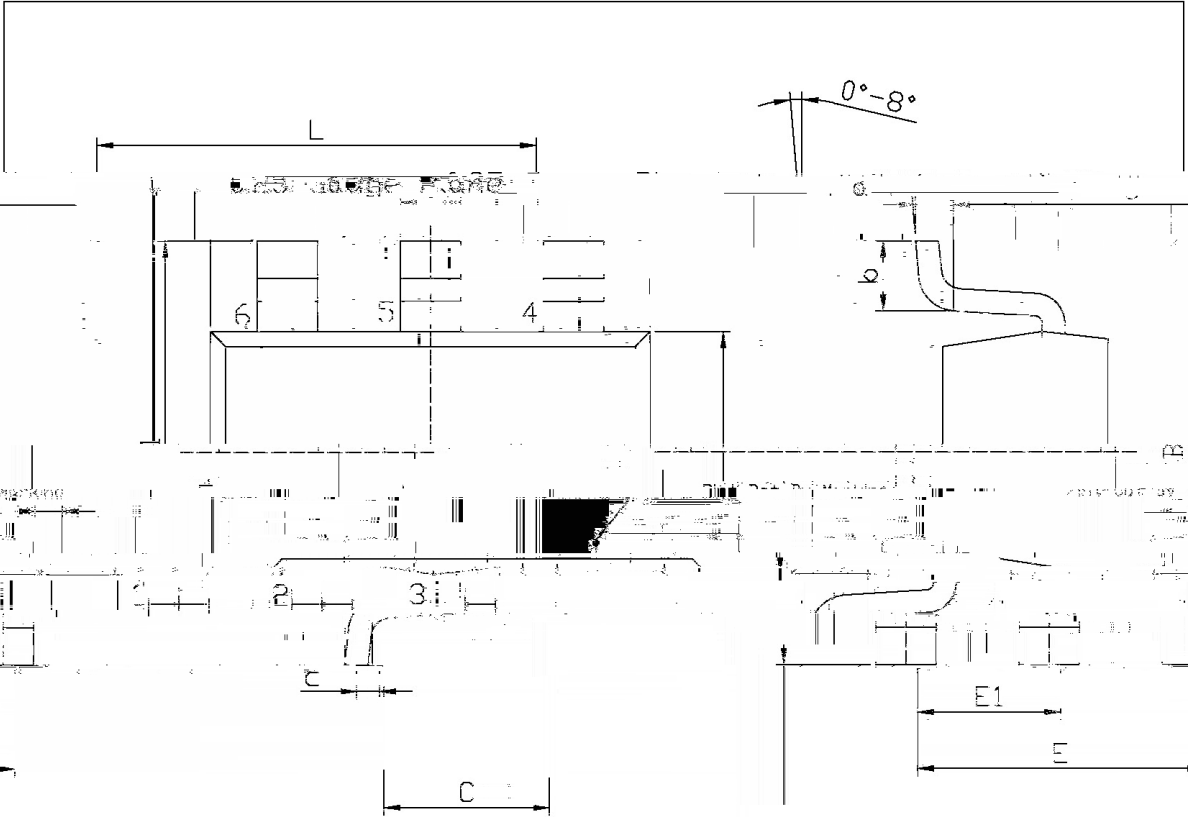
		°C

/ Electrical Characteristics(Ta=25 VDD=20V if not otherwise noted)

VDD						
FB						
Δ						
DRV						

/ Functional Description

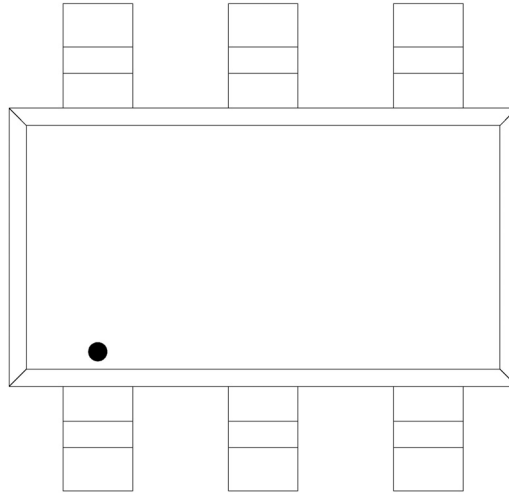
/ Package Dimensions



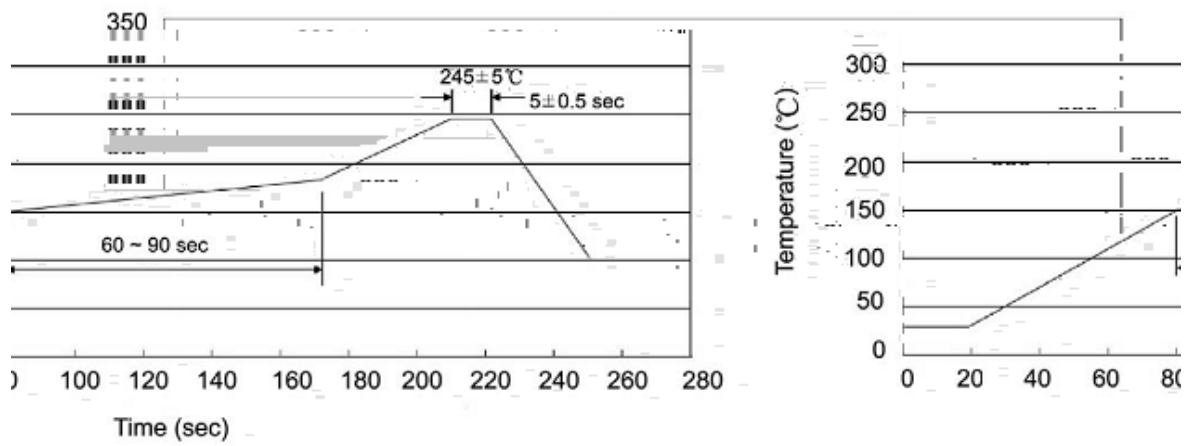
Unit: mm					
Dimensions In Millimeters			Dimensions In Millimeters		
Symbol	Min	Max	Symbol	Min	Max
L	2.82	3.02	E1	0.85	1.05
B	1.50	1.70	a	0.35	0.50
C	0.90	1.30	c	0.10	0.20
L1	2.60	3.00	b	0.35	0.55
E	1.80	2.00	F	0	0.15

SOT23-6

/ Marking Instructions



() / Temperature Profile for IR Reflow Soldering(Pb-Free)



/ Resistance to Soldering Heat Test Conditions

/ Packaging SPEC.

/ Notices